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L4	L3 and (electroplat\$6 or electroly\$6 or electrochem\$6 or electrodeposit\$6)	276	L4
L3	L2 and (copper or cu)	783	L3
L2	L1 and ((remov\$6 or wip\$6 or brush\$6 or sweep\$6 or swab\$6 or scrap\$6 or pad46 or rub\$6 or buff\$6 or polish\$6) near8 (additive\$3 or suppressor\$3 or accelerator\$3 or leveler\$3 or brightener\$3 or wetting or surfactant\$3))	4125	L2
L1	(additive\$3 or suppressor\$3 or accelerator\$3 or leveler\$3 or brightener\$3 or wetting or surfactant\$3) near10 (via\$3 or hole\$3 or feature\$3 or channel\$3 or opening\$3 or trench\$3 or cavit\$6 or passage\$5)	35321	L1

END OF SEARCH HISTORY

Patent Assignment Abstract of Title

Total Assignments: 1**Application #:** 09961193 **Filing Dt:** 09/20/2001**Patent #:** NONE**Issue Dt:****PCT #:** NONE**Publication #:** NONE**Pub Dt:****Inventor:** Bulent M. Basol**Title:** Plating method and apparatus for controlling deposition on predetermined portions of a workpiece**Assignment: 1**

Reel/Frame: <u>012510/0039</u>	Received: 01/30/2002	Recorded: 01/22/2002	Mailed: 03/25/2002	Pages: 2
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Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).**Assignor:** BASOL, BULENT**Exec Dt:** 12/04/2001**Assignee:** NUTOOL, INC.1645 MCCANDLESS DRIVE
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Web interface last modified: Oct. 5, 2002

WEST

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L4: Entry 274 of 276

File: JPAB

Oct 19, 2001

PUB-NO: JP02001291954A
DOCUMENT-IDENTIFIER: JP 2001291954 A
TITLE: VIA-FILLING PLATING METHOD

PUBN-DATE: October 19, 2001

INVENTOR-INFORMATION:

NAME

COUNTRY

NAKAMURA, KENJI

NAKAZAWA, MASAO

ASSIGNEE-INFORMATION:

NAME

COUNTRY

SHINKO ELECTRIC IND CO LTD

APPL-NO: JP2000334044

APPL-DATE: November 1, 2000

INT-CL (IPC): H05 K 3/42; H05 K 3/18; H05 K 3/40; H05 K 3/46

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a via-filling plating method capable of satisfactorily filling even the via hole of a large aspect ratio and a small diameter with copper plating.

Seed
Removing
accelerator
SOLUTION: This method is provided with a copper coating forming process for forming copper coating 21 on the wall surface of a substrate 20, including the front surface of an insulating layer 12 and the bottom surface of a via hole 14, an immersing process for sticking a plating accelerator on the surface of copper coating 21 by immersing the substrate 20 formed with copper coating 21 in an aqueous solution added with the plating accelerator, a releasing process for removing the plating accelerator 22 stuck on the surface of copper coating 21 except for the inner wall surface including the bottom surface of the via hole 14, and an electrolytic copper plating process for filling the via hole 14 with a plating metal by applying electrolytic copper plating onto copper coating 21, formed on the surface of the insulating layer 12 and on the wall surface including the bottom surface of the via hole 14 after the releasing process.

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